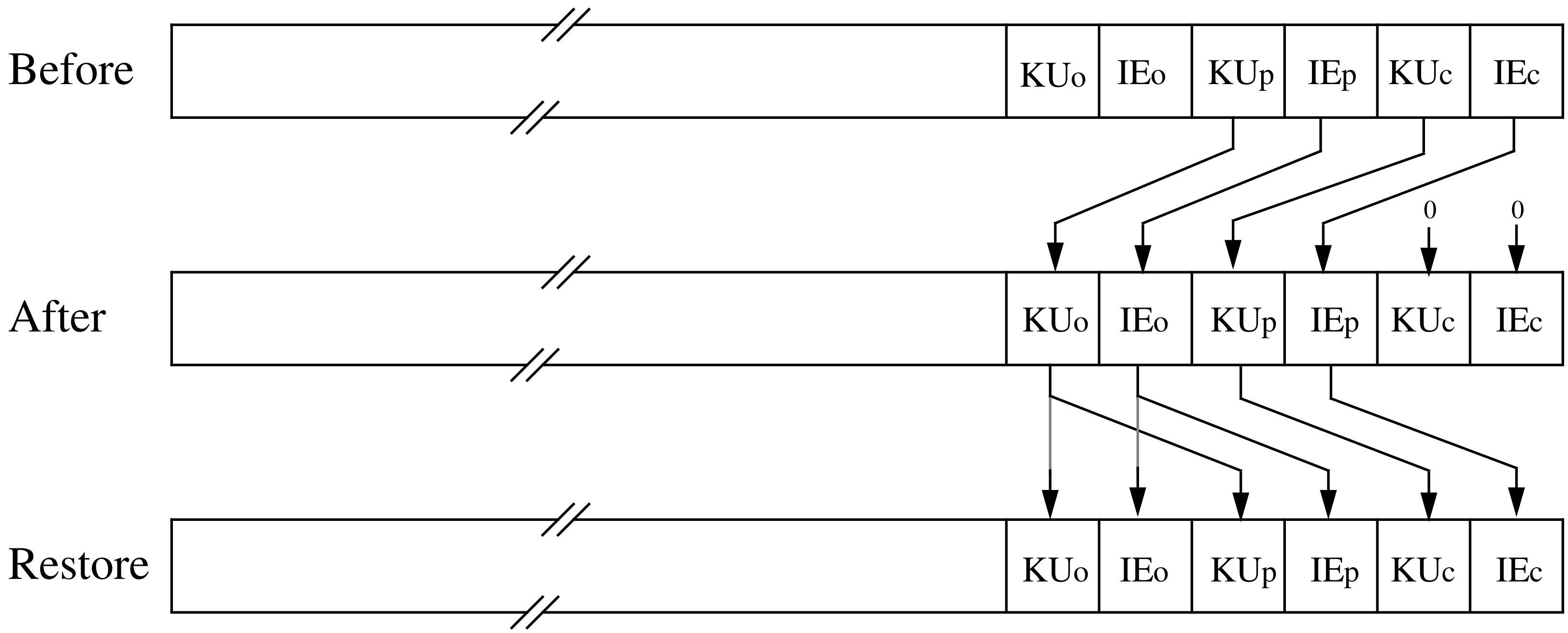
EXCEPTION HANDLING

STATUS REGISTER



- Current Previous Old
- KU = Kernel/User IE = Int Enable

STATUS REGISTER

										KU & IE		
CU	0	BEV	TS	PE	CM	PZ	CACHE CNTL	INT MASK	0	OLD	PREV	CUR
4	5						2	8	2	2	2	2

CU	Coprocessor Usability
BEV	Bootstrap Exception Vector
TS	TLB Shutdown
PE	Parity Error
CM	Cache Miss
PZ	Parity Zero
CACHE CNTL	Swap & Isolate
INT MASK	Int5..0 & SW1..0

CACHE CONTROL

ISOLATE CACHE:

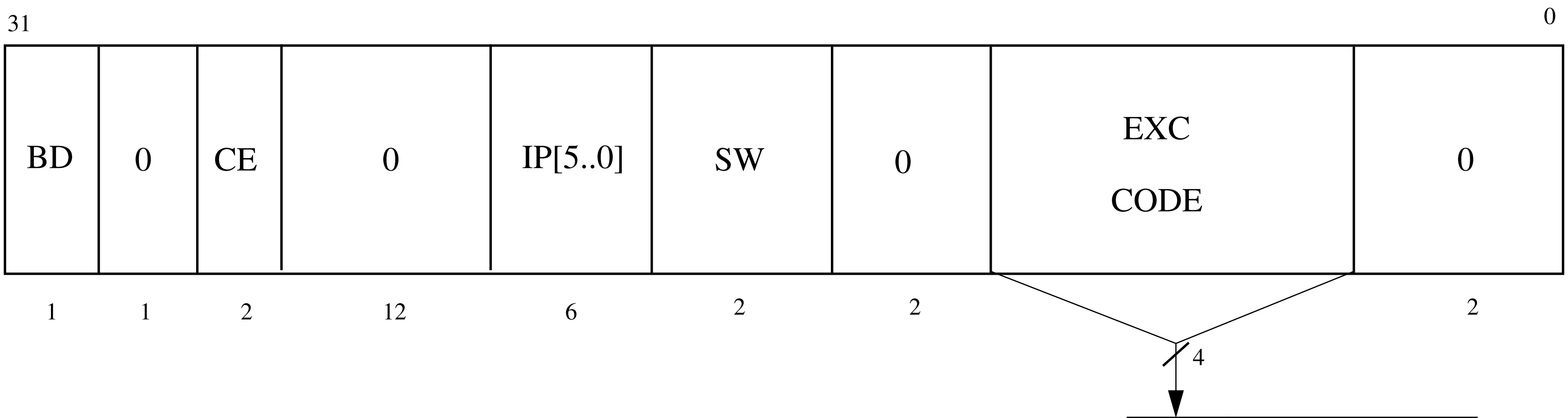
- Inhibits MemRd* and MemWr*, i.e. Cache Only.
- Causes All Partial Word Writes to Clear Cache Valid Bit.

SWAP CACHES:

- Causes All Data Accesses to use I-Cache (IWr* & IRd*) and All Instruction Accesses to use D-Cache (DWr* & DRd*).

- Used for Initialization, Testing and Diagnostics

CAUSE REGISTER



0	INT
1	MOD
2	TLBL
3	TLBS
4	AdEL
5	AdES
6	IBE
7	DBE
8	Sys
9	BP
10	RI
11	CpU
12	Ovf
13-15	RSVD

BD	Branch Delay
CE	Coprocessor Error
IP	Interrupts Pending
SW	S/W Interrupts Pending

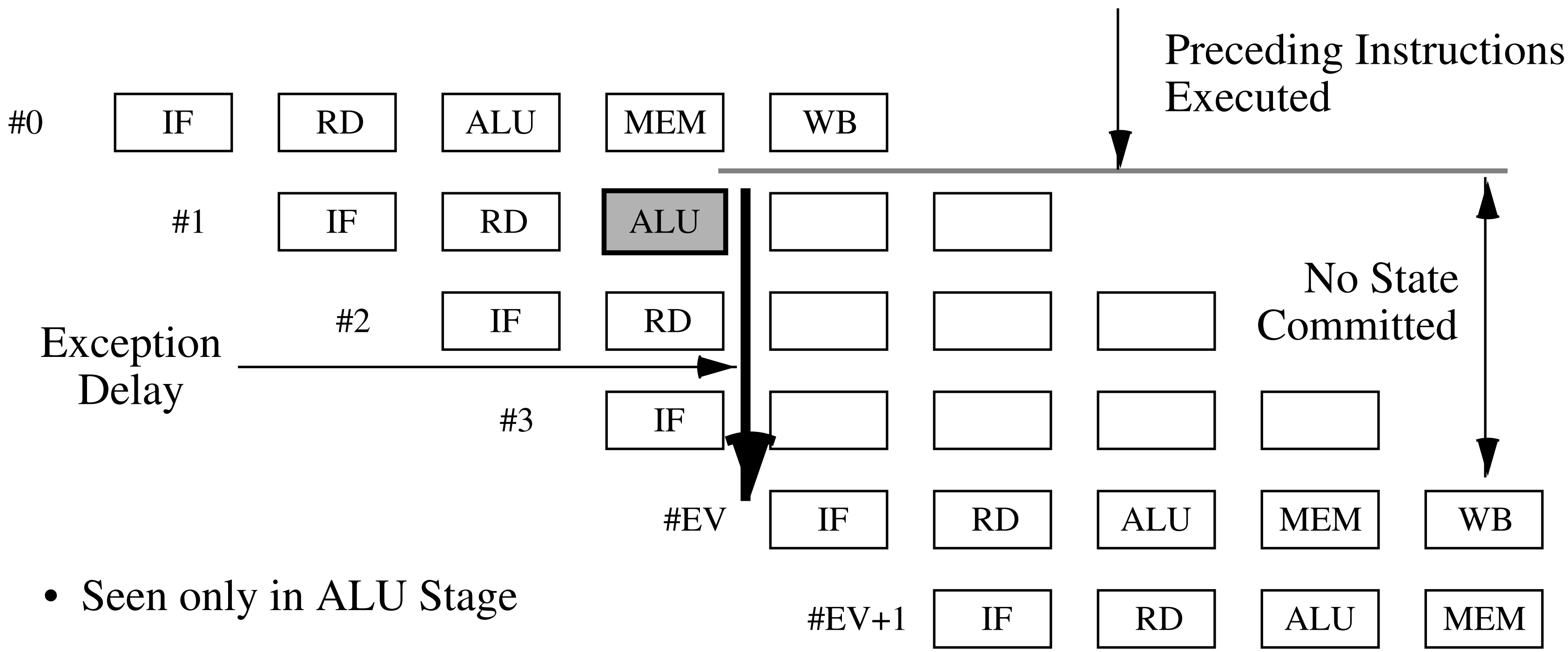
EXCEPTION VECTORS

TYPE	HANDLER BEV=1	HANDLER BEV=0	CAUSE
RESET	BFC0_0000	BFC0_0000	ASSERTION OF RESET PIN
UTLB	BFC0_0100	8000_0000	USER TLB MISS
TLBL TLBS			TLB MISS LOAD TLB MISS STORE
MOD			TLB MODIFIED
IBE DBE			BUS ERROR INSTR BUS ERROR DATA
AdEL AdES	BFC0_0180	8000_0080	ADDRESS ERROR LOAD ADDRESS ERROR STORE
Ovf Sys			OVERFLOW SYSTEM CALL
BP RI			BREAK POINT RESERVED INSTR
CpU INT			COPROCESSOR UNUSABLE HARDWARE INTERRUPT

INTERRUPTS

- Sampled in Phase 2 of all Run and Fixup Cycles
- Hardware Interrupts must be Held Until Serviced
- Stall Will Prevent Interrupt Exception
- Maskable

INTERRUPTS (SERVICE START)



- Seen only in ALU Stage
- EPC := PC or PC-4
- PC Loaded with EV Address
- KU & IE Bits Updated

INTERRUPTS (LATENCY CALCULATION)

Latency = t response + t savestatus + t vector

t response	t savestatus	t vector
Finish Current Operation	Save Processor State	Jump to Routine

INTERRUPTS
(LATENCY CALCULATION EXAMPLE)

t response:

t response (min) = 1 cycle

t response (max) = 35 cycles (longest* stall -- integer divide)

t vector:

t vector (min) = t vector (max) = 2 cycles

* Assuming Memory System Doesn't Produce a Longer Stall !

INTERRUPTS
(LATENCY CALCULATION EXAMPLE)

t savestatus:

t savestatus (min) = 1 + 1 + 31 + 2 = 35* cycles (instructions)

Disable Interrupts | Save SR | Save Registers | Save HI & LO

t savestatus (max) = t savestatus (min) with Cache Miss Penalty**

= (35/16 * 12) + (35/4 * (12 + 1)) + 35

Refill Size | Stores | WB Depth | Fixup | Memory Latency

= 36 + 104 + 35 = 175 cycles

* May not Need to save *Any* Register

** Numbers Based on M2000 Design

INTERRUPT LATENCY

Best Case Latency = Sum of Minimums of Components

= 1 + 35 + 2 = 38 cycles
= 1.5 s at 25MHz

= 1 + 1 + 2 = 4 cycles
= 160ns at 25MHz

Worst Case Latency = Sum of Maximums of Componenents

= 35 + 175 + 2 = 212 cycles

= 8.5 s at 25MHz

- Typical Latency will Usually be Closer to the Minimum Number