MIPS R4400Master_Checker Errata, Processor Revision 1.0

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"Master/Checker Mode" is used when two R4400s are operated in the lock step. For detail explanation of this mode see "MIPS R4400 Features" document. Additional errata which affect PC or SC designs are listed in the "MIPS R4400 PC, R4400SC Errata". Change bars in the left column indicate corrections or changes from the last version of the errata.

1. Processors might not function in "lock-step" properly because the timer in CP0 (Count Register) may not synchronize across multiple processors at reset. As a result, the timers may increment on different clock edges across multiple parts causing either a timer interrupt to occur on a different cycle, or the value read from the count register to be off by one least significant bit.

Workaround: Do not use the Count Register as a timer when running in the master/checker mode..

2. The two chips running in the master/checker mode may go out of step, due to a circuit hazard in accessing the cache, under following condition:

Condition: As a result of a jump or eret instruction, there is a switch from unmapped to mapped space and the processor takes a TLB refill exception due to a miss at the destination address.

Symptom: The "out of step" behavior may appear, during the SCache access, as one extended cycle.

The operation of the processor is not affected by this behavior. User programs will work properly since they are normally run from the mapped space. However, the kernel must avoid the situation, discussed above, from occurring.

Workaround: When jump or eret switches the operation from unmapped to mapped space then the line in the line primary ICache that maps to the destination must be marked invalid. This can be done by using the Cache Index Invalidate instruction for the destination index address and also making sure that the jump or eret is not at the same cache index address as the destination index address.